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06EC46

Fourth Semester B.E. Degree Examination, June/July 2011
Linear ICs and Applications

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain common mode voltage, common mode voltage gain and common mode rejection ratio for operational amplifiers. Show that $V_{0(cm)} = \frac{V_{i(cm)}}{CMRR} \times A_v$ **(10 Marks)**

b. With a neat circuit diagram, explain direct-coupled non-inverting amplifier with necessary design steps. **(05 Marks)**

c. Sketch an op-amp difference amplifier circuit. Derive an equation for the output voltage and explain the operation. **(05 Marks)**

2 a. Explain the operation of a high input impedance capacitor-coupled non-inverting amplifier with a neat circuit diagram. **(10 Marks)**

b. A capacitor-coupled non-inverting amplifier is to have a +24V supply, a voltage gain of 100, an output amplitude of 5V, a lower cutoff frequency of 75 Hz and a minimum load resistance of 5.6 kΩ. Using a 741 op-amp, design a suitable circuit. Given: $I_{B(max)}$= 500 nA, f_1 = 75 Hz, R_L = 5.6 kΩ **(10 Marks)**

3 a. Discuss the different frequency compensating methods with the circuit diagrams. Also show how each one of them affect the frequency response of an op-amp. **(12 Marks)**

b. Calculate the slow-rate limited cutoff frequency for a voltage follower circuit using a 741 op-amp, if the peak of sinewave output is to be 5 V. Determine the maximum peak value of the sinusoidal output voltage that will allow the 741 voltage follower circuit to operate at 800 kHz unity-gain cutoff frequency. Given : S = 0.5 V/μs. **(05 Marks)**

c. Calculate the cut-off frequency-limited risetime for a voltage follower circuit using a 741 op-amp. Also, determine the slow rate-limited risetime if the output amplitude is to be 5V. Given: S = 0.5 V/μs, f_2 = 800 kHz. **(03 Marks)**

4 a. Show how two op-amp dead zone circuits can be combined with a summing circuit to produce precision limiting on both positive and negative half-cycles of the output waveform. Draw the voltage waveforms through out the circuit and explain its operation. **(10 Marks)**

b. Design a precision voltage source to provide an output of 9 V. The available supply is ±12V. Allow for approximately ±10% tolerance on the zener diode voltage. Use 741 op-amp. Given : $I_{B(max)}$ = 500 nA, I_z = 20 mA. **(10 Marks)**

PART – B

5 a. With a neat circuit diagram, explain the operation of a precision rectifier peak detector circuit. Draw the input and output waveforms. Write the equation for calculating the capacitor value. **(08 Marks)**

b. With a neat circuit diagram, explain the operation of a Log amplifier using op-amp. Derive the output voltage equation. **(06 Marks)**

c. Using a 741 op-amp, with a supply of $\pm$12V, design a phase-shift oscillator to have an output frequency of 3.5 kHz. Given $I_{B(max)} = 500$ nA. **(06 Marks)**

6 a. With neat circuit diagrams, explain how diodes may be used to select the trigger points of an inverting Schmitt trigger circuit. **(06 Marks)**

b. With a neat circuit diagram and waveforms, explain the operation of op-amp based astable multivibration. Write the design steps. **(08 Marks)**

c. Design a second-order low-pass filter circuit to have a cutoff frequency of 1 kHz. **(06 Marks)**

7 a. Define the following performance parameters of a voltage regulator;
Line regulation, Load regulation, Ripple rejection. **(06 Marks)**

b. With a neat functional diagram, explain the operation of a low-voltage regulator using IC723. **(08 Marks)**

c. Bring out the limitations of Linear voltage regulators. **(06 Marks)**

8 a. Explain the working of monostable multivibrator using 555 timer with a neat functional diagram and waveforms. Derive the equation for its pulse width. **(08 Marks)**

b. Draw the block diagram representation of PLL and explain. **(06 Marks)**

c. With a neat circuit diagram and staircase waveform, explain the operation of counter type Analog-to-Digital converter. **(06 Marks)**

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